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Key Specifications

Processor Core
- 800 MHz A7 core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache
- 1.25GHz A17 core, supporting 32 KB I-cache, 32 KB D-cache, and 256 KB L2 cache
- Neon acceleration, integrated FPU
- ARM@big-LITTLE architecture

Video Encoding
- H.264 BP/MP/HP
- H.265 Main Profile
- MJPEG/JPEG baseline encoding
- I/P/B frame, dual-P-frame reference
- CBR, VBR, FIXQP, AVBR, and QPMAP modes
- Maximum 16-megapixel (4608 x 3456) resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capability: 3840 x 2160@30 fps + 1080p@30 fps + 3840 x 2160@2fps snapshot
- Maximum JPEG snapshot performance of 3840 x 2160@30 fps
- CBR, VBR, FIXQP, AVBR, and QPMAP modes
- Maximum100 Mbit/s output bit rate
- Encoding of eight ROIs

Intelligent Video Analysis
- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing
- 3D denoising, image enhancement, and dynamic contrast improvement
- Anti-flicker for output videos and graphics
- 1/30x to 16x video scaling
- Seamless splicing of 2-channel videos
- 1/2x to 2x graphics scaling
- OSD overlaying of eight regions before encoding
- Video graphics overlaying of two layers (video layer and graphics layer)

ISP
- 2-channel independent ISP processing
- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilization
- Anti-fog
- Lens distortion correction and fisheye correction
- Picture rotation by 90° or 270°
- Picture mirroring and flipping
- Sensor built-in WDR, 4F/3F/2F frame-based/line-based WDR, and local tone mapping. The second channel of ISP processing supports only sensor built-in WDR, 2F frame-based/line-based WDR, and local tone mapping.
- ISP tuning tools for the PC

Audio Encoding/Decoding
- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726 and ADPCM protocols
- Audio 3A functions (AEC, ANR, and ALC)

Security Engine
- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA1024/2048/4096 signature verification algorithm implemented by using hardware
- Hash-SHA1/256 and HMAC_SHA1/256 tamper proofing algorithms implemented by using hardware
- Integrated 512-bit OTP storage space and hardware random number generator

Video Interfaces
- VI Interfaces
  - Two sensor inputs. The maximum resolution for the main channel is 16 megapixels (4608 x 3456), and the maximum resolution for the second input is 8 megapixels (4096 x 2160).
  - 8-/10-/12-/14-bit RGB Bayer DC timing VI, at most 150 MHz clock frequency
  - BT.601, BT.656, or BT.1120 VI interface
  - Maximum 12-lane MIPI/LVDS/sub-LVDS/HiSPI interface for the main channel
  - Maximum 4-lane MIPI/LVDS/sub-LVDS/HiSPI interface for the second sensor interface
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
- VO interfaces
  - One PAL/NTSC output for automatic load detection
  - One BT.1120/BT.656 VO interface for connecting to an external HDMI or SDI, supporting at most 1080p@60 fps output
  - LCD output

Audio Interfaces
- Integrated audio CODEC supporting 16-bit audio inputs and outputs
- IFS interface for connecting to an external audio CODEC
- Dual-channel differential MIC inputs for reducing background noises

Peripheral Interfaces
- POR
- External reset input
- Internal RTC
- Integrated 3-channel LSADC
Hi3519 V101 Professional HD IP Camera SoC

- Five UART interfaces
- IR interface, I2C interface, SSP master interface, and GPIO interface
- Eight PWM interfaces (four independent interfaces and four ones multiplexed with other pins)
- Two SD 3.0/SDIO 3.0 interfaces, supporting SDXC
- One USB 3.0/USB 2.0 host/device port
- One PCIe 2.0 interface in master/slave mode
- RGMII/RMII in 10/100 Mbit/s full-/half-duplex mode and 1000 Mbit/s full-duplex mode, and TSO network acceleration

External Memory Interfaces
- DDR4/DDR3/DDR3L/LPDDR3 interface
  - 32-bit LPDDR3 interface with the maximum frequency of 800 MHz (1.6 Gbit/s)
  - 32-bit DDR4/3/3L interface with the maximum frequency of 933 MHz (1.866 Gbit/s)
  - Maximum capacity of 1024 MB for a 16-bit DDR SDRAM
  - Maximum total capacity of 2048 MB for two 16-bit DDR SDRAMs
- SPI NOR flash interface
  - 1-/2-/4-wire mode
  - 3-byte or 4-byte address mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface, supporting the maximum capacity of 512 MB
- eMMC 5.0 interface, supporting the maximum capacity of 2 TB
- NAND flash interface
  - 8-bit data width
  - SLC or MLC
  - 4-/8-/24-/40-/64-bit ECC
  - Components with 8 GB or larger capacity
- Booting from the SPI NOR flash, SPI NAND flash, or NAND flash
- Booting from an eMMC or over PCIe

SDK
- Linux-3.18-based SDK
- High-performance H.265 PC/iOS/Android decoding library
- High-performance H.264 PC decoding library

Physical Specifications
- Power consumption
  - 1.5 W typical power consumption
  - Multi-level power saving mode
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
  - 1.2 V, 1.5 V, 1.35 V, or 1.2 V DDR4/3/3L/LPDDR3 SDRAM interface voltage
- Package
  - RoHS, FC-CSP
  - Body size of 10 mm x 10 mm (0.39 in. x 0.39 in.)
  - Lead pitch of 0.4 mm (0.02 in.)
As a new-generation industry-specific SoC designed for the HD IP camera, Hi3519 V101 integrates a new-generation ISP and uses the latest H.265 video compression encoder in the industry as well as advanced low-power technology and architecture design. These features enable Hi3519 V101 to continuously maintain the leading position in the aspects of low bit rate, high picture quality, and low power consumption. Hi3519 V101 supports 90° or 270° rotation and lens distortion correction by using hardware, which meet requirements in various surveillance application scenarios. It also supports 3A algorithms, which allow customers to design various models of IP cameras that contain integrated camera cores. Hi3519 V101 integrates the POR, RTC, and audio CODEC and supports various sensor levels and clock outputs, which significantly reduces the EBOM cost of the HD IP camera based on Hi3519 V101. The Hi3519 V101 HiSilicon SDK features high stability and ease of use, supports rapid mass production, and facilitates system layout of DVRs, NVRs, and IP cameras.
Acronyms and Abbreviations

3DES  triple data encryption standard
ADC  analog-to-digital converter
ADPCM  adaptive differential pulse code modulation
AE  automatic exposure
AEC  acoustic echo cancellation
AES  advanced encryption standard
AF  automatic focus
ALC  automatic level control
ANR  active noise reduction
AWB  automatic white balance
CBR  constant bit rate
CMOS  complementary metal-oxide-semiconductor
CODEC  coder/decoder
DCI  dynamic contrast improvement
DDR  double data rate
DES  data encryption standard
DPC  defect pixel correction
DVR  digital video recorder
EBOM  engineering bill of materials
ECC  error correcting code
eMMC  embedded multimedia card
FD  face detection
FPN  fixed pattern noise
FPU  floating-point unit
GPIO  general-purpose input/output
HD  high definition
HDMI  high definition multimedia interface
HiSPi  high-speed serial pixel interface
I²C  inter-integrated circuit
I²S  inter-IC sound
IR  infrared
ISP  image signal processor
IVE  intelligent video engine
LCD  liquid crystal display
LDC  lens distortion correction
LVDS  low-voltage differential signaling
MIC  microphone
MIPI  mobile industry processor interface
MLC  multi-level cell
NTSC  National Television System Committee
NVR  network video recorder
OSD  on-screen display
OTP  one-time programming
PAL  phase alternating line
PCle  peripheral component interconnect express
POR  power-on reset
PWM  pulse-width modulation
RGMII  reduced gigabit media independent interface
RMII  reduced media independent interface
RoHS  Restriction of Hazardous Substances
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
</tr>
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<tbody>
<tr>
<td>ROI</td>
<td>region of interest</td>
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<tr>
<td>RSA</td>
<td>Rivest-Shamir-Adleman</td>
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<tr>
<td>RTC</td>
<td>real-time clock</td>
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<tr>
<td>SAR</td>
<td>successive approximation register</td>
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<tr>
<td>SD</td>
<td>secure digital</td>
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<tr>
<td>SDI</td>
<td>serial digital interface</td>
</tr>
<tr>
<td>SDIO</td>
<td>secure digital input/output</td>
</tr>
<tr>
<td>SDK</td>
<td>software development kit</td>
</tr>
<tr>
<td>SDRAM</td>
<td>synchronous dynamic random access memory</td>
</tr>
<tr>
<td>SDXC</td>
<td>secure digital extended capacity</td>
</tr>
<tr>
<td>SLC</td>
<td>single-level cell</td>
</tr>
<tr>
<td>SoC</td>
<td>system-on-chip</td>
</tr>
<tr>
<td>SPI</td>
<td>serial peripheral interface</td>
</tr>
<tr>
<td>SSP</td>
<td>synchronous serial port</td>
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<tr>
<td>TFBGA</td>
<td>thin fine ball grid array</td>
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<tr>
<td>TSO</td>
<td>TCP segmentation offload</td>
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<tr>
<td>UART</td>
<td>universal asynchronous receiver transmitter</td>
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<tr>
<td>VBR</td>
<td>variable bit rate</td>
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<tr>
<td>VDMA</td>
<td>virtual direct memory access</td>
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<tr>
<td>VI</td>
<td>video input</td>
</tr>
<tr>
<td>VO</td>
<td>video output</td>
</tr>
<tr>
<td>WDR</td>
<td>wide dynamic range</td>
</tr>
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