Hi3520D V400 H.265 Codec Processor

Brief Data Sheet

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Key Specifications

**Processor Core**
- ARM Cortex A7 dual-core@maximum 1.3 GHz
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 256 KB L2 cache
  - NEON and FPU

**Video Encoding/Decoding Protocols**
- H.265 Main Profile, Level 4.1 encoding
- H.265 Main Profile, Level 4.1 decoding
- H.264 Baseline/Main/High Profile, Level 4.2 encoding
- H.264 Baseline/Main/High Profile, Level 4.2 decoding
- MPEG-4 SP, L0–L3/ASP L0–L5 decoding
- MJPEG/JPEG baseline

**Video Encoding/Decoding**
- H.265/H.264/JPEG encoding and decoding of multiple streams
  - 4x1080p@15fps H.265/H.264 encoding+4xD1@15fps
  - H.265/H.264 encoding+4x1080p@15fps H.265/H.264 decoding+4x1080p@2fps JPEG encoding
  - 4x720p@30fps H.265/H.264 encoding+4xD1@30fps
  - H.265/H.264 encoding+4x720p@30fps H.265/H.264 decoding+4x720p@2fps JPEG encoding
- Constant bit rate (CBR) mode, variable bit rate (VBR) mode, FIXQP mode, adaptive variable bit rate (AVBR) mode, and QpMap mode
- Maximum 40 Mbit/s output bit rate
- ROI encoding
- Color-to-gray encoding

**Intelligent Video Analysis**
- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

**Video and Graphics Processing**
- Deinterlacing, sharpening, 3D denoising, dynamic contrast improvement, and demosaic
- Anti-flicker for output videos and graphics
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- Four Cover regions
- OSD overlaying of eight regions

**Audio Encoding/Decoding**
- ADPCM, G.711, and G.726 hardware audio encoding
- Software audio encoding and decoding complying with multiple protocols

**Security Engine**
- AES, DES, and 3DES algorithms implemented by hardware

**Video Interfaces**
- VI interfaces
  - Two 8-bit interfaces or one 16-bit interface
  - 108 MHz/144 MHz 4xD1/960H TDM inputs for each 8-bit interface (8xD1/8x960H real-time video inputs in total)
- 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (4x720p@30 fps real-time video inputs in total)
- 4x720p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (8x720p@30 fps real-time video inputs in total)
- 148.5 MHz BT.1120 inputs in Y/C interleaved mode for each 8-bit interface (2x1080p@30 fps real-time video inputs in total)
- 2x1080p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (4x1080p@30 fps real-time video inputs in total)
- 148.5 MHz BT.1120 standard mode for the 16-bit interface (1x1080p@60 fps real-time video inputs in total)
- VO interfaces
  - One HDMI 1.4b output interface with the maximum output of 3840 x 2160@30 fps
  - One VGA HD output interface with the maximum output of 1080p@60 fps
  - Two independent HD output channels (DHD0 and DHD1), output over any HD interface (HDMI or VGA)
  - 16-picture output for DHD0, maximum output of 3840 x 2160@30 fps
  - 16-picture output for DHD1, maximum output of 1080p@60 fps
  - One CVBS SD output interface
  - Three full-screen GUI graphics layers in ARGB1555 or ARGB8888 format for two HD channels and one SD channel
  - Two hardware cursor layers in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256

**Audio Interfaces**
- Three unidirectional I²S/PCM interfaces
  - Two input interfaces, supporting 16 multiplexed inputs
  - One output, supporting dual-channel output
  - 16-bit audio inputs and outputs

**Ethernet Ports**
- One gigabit Ethernet port
  - RGMII, RMII, and MII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU usage

**Peripheral Interfaces**
- Two SATA 3.0 interfaces
  - PM
  - eSATA
- Two USB 2.0 host ports, supporting the hub
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- Three UART interfaces, one of which supporting four wires
- One SPI, supporting two CSs
- One IR interface
- One I²C interface
- Multiple GPIO interfaces

**Memory Interfaces**
- One 16-bit DDR3 SDRAM interface
  - Maximum frequency of 800 MHz
  - ODT
  - Maximum capacity of 1 GB
  - Automatic power consumption control
- SPI NOR/NAND flash interface
  - 1-/2-/4-wire SPI NOR/NAND flash
  - Two CSs, connected to different types of flash memories
  - Maximum capacity of 64 MB for each CS (for the SPI NOR flash)
  - Maximum capacity of 512 MB for each CS (for the SPI NAND flash)
  - 2 KB/4 KB page size (for the SPI NAND flash)
  - 8-bit/1 KB or 24-bit/1 KB ECC (for the SPI NAND flash)
- Embedded 4 KB BOOTROM and 16 KB SRAM

**RTC with an Independent Power Supply**
- Independent battery for supplying power to the RTC

**Configurable Boot Modes**
- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash

**SDK**
- Linux 3.18-based SDK
- Audio encoding and decoding libraries complying with various protocols
- High-performance H.265/H.264 PC decoding library

**Physical Specifications**
- Power consumption
  - Typical power consumption of 2.0 W
  - Multi-level power consumption control
- Operating voltages
  - 0.9 V core voltage
  - 1.0 V CPU voltage
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Package
  - RoHS, TFBGA
  - Lead pitch of 0.65 mm (0.03 in.)
  - Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)
The Hi3520D V400 is a professional SoC targeted for the multi-channel HD (1080p/720p) or SD (D1/960H) DVR. The Hi3520D V400 provides an ARM A7 dual-core processor, a high-performance H.265/H.264 video encoding/decoding engine, a high-performance video/graphics processing engine with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable the Hi3520D V400 to provide high-performance, high-picture-quality, and low-cost analog HD/SDI solutions for customers' products while reducing the eBOM cost.

**DVRs (Each with a Hi3520D V400)**

**4x1080p Non-Real-Time DVR**
- 4x1080p@15 fps H.265 encoding+4xD1@15 fps H.265 encoding+4x1080p@15 fps H.265 decoding+4x1080p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

**4x720p DVR**
- 4x720p@30 fps H.265 encoding+4xD1@30 fps H.265 encoding+4x720p@30 fps H.265 decoding+4x720p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs
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Hi3520D V400

- 2x4M or 4x1080p or 8x720p CHs. A/V Dec.
- HDMI (1080p)
- VGA (1080p)
- CVBS
- SATA
- SATA
- SATA
- SATA
- USB2.0 Host
- Flash
- DDR3
- GE PHY
- LAN/WAN
- FMC
- DDR Ctrl
- GMAC
- VI0
- VI1
- I2S0
- I2S1
- I2S2

Hi3520DV400
Acronyms and Abbreviations

3DES triple data encryption standard
ADPCM adaptive differential pulse code modulation
AES advanced encryption standard
CBR constant bit rate
CS chip select
CVBS composite video broadcast signal
DCI dynamic contrast improvement
DDR double data rate
DES data encryption standard
DVR digital video recorder
eBOM engineering bill of materials
ECC error correcting code
eSATA external serial advanced technology attachment
GPIO general-purpose input/output
HD high definition
HDMI high definition multimedia interface
I²C inter-integrated circuit
I²S inter-IC sound
IR infrared
IVE intelligent video engine
MII media independent interface
ODT on-die termination
OSD on-screen display
PCM pulse code modulation
PM port multiplexer
QP quantization parameter
RGMII reduced gigabit media independent interface
RMII reduced media independent interface
RoHS Restriction of Hazardous Substances
ROI region of interest
RTC real-time clock
SATA serial advanced technology attachment
SD standard definition
SDI serial digital interface
SDK software development kit
SDRAM synchronous dynamic random access memory
SoC system-on-chip
SPI serial peripheral interface
SRAM static random access memory
TDM time division multiplexing
TSO TCP segmentation offload
UART universal asynchronous receiver transmitter
VBR variable bit rate
VGA video graphics array
VI video input
VO video output