Hi3521D V100 H.265 CODEC Processor

Brief Data Sheet

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Key Specifications

Processor Core
- ARM Cortex A7 dual-core@maximum 1.3 GHz
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 256 KB L2 cache
  - NEON and FPU

Video Encoding/Decoding Protocols
- H.265 Main Profile, Level 5.0 encoding
- H.265 Main Profile, Level 5.0 decoding
- H.264 Baseline/Main/High Profile, Level 5.1 encoding
- H.264 Baseline/Main/High Profile, Level 5.1 decoding
- MPEG-4 SP, L0–L3/ASP L0–L5 decoding
- MJPEG/JPEG baseline

Video and Graphics Processing
- Deinterlacing, sharpening, 3D denoising, dynamic contrast improvement, and deemscing
- Anti-flicker for output videos and graphics
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- Four Cover regions
- OSD overlaying of eight regions

Audio Encoding/Decoding
- ADPCM, G.711, and G.726 hardware audio encoding
- Software audio encoding and decoding complying with multiple protocols

Security Engine
- AES, DES, and 3DES algorithms implemented by hardware

Video Interfaces
- V1 interfaces
  - Four 8-bit interfaces or two 16-bit interfaces
  - 108 MHz/144 MHz 4x1D/960H TDM inputs for each 8-bit interface (16xD1/16x960H real-time video inputs in total)
  - 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (8x720p@30 fps real-time video inputs in total)
  - 4x720p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (16x720p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 Y/C interleaved mode for each 8-bit interface (4x1080p@30 fps real-time video inputs in total)
  - 2x1080p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (8x1080p@30 fps real-time video inputs in total)
  - 1x4M (2560 x 1440) TDM inputs through 148.5 MHz dual-edge or 297 MHz single-edge sampling for each 8-bit interface (4x4M@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 standard mode for the 16-bit interface (2x1080p@60 fps real-time video inputs in total)

- VO interfaces
  - One HDMI 1.4b output interface with the maximum output of 3840 x 2160@30 fps
  - One VGA HD output interface with the maximum output of 1080p@60 fps
  - Two independent HD output channels (DHD0 and DHD1), output over any HD interface (HDMI or VGA)
  - 36-picture output for DHD0, maximum output of 3840 x 2160@30 fps
  - 16-picture output for DHD1, maximum output of 1080p@60 fps
  - One CVBS SD output interface
  - Three full-screen GUI graphics layers in ARGB1555 or ARGB8888 format for two HD channels and one SD channel
  - Two hardware cursor layers in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256

Audio Interfaces
- Three unidirectional I2S/PCM interfaces
  - Two input interfaces, supporting 16 multiplexed inputs
  - One output, supporting dual-channel output
  - 16-bit audio inputs and outputs
Hi3521D V100 Ethernet Ports
- One gigabit Ethernet port
  - RGMII, RMII, and MII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU usage

Peripheral Interfaces
- Two SATA 3.0 interfaces
  - PM
  - eSATA
- Two USB 2.0 host ports, supporting the hub
- Three UART interfaces, one of which supporting four wires
- One SPI, supporting two CSs
- One IR interface
- One I2C interface
- Multiple GPIO interfaces

Memory Interfaces
- One 32-bit DDR3 SDRAM interface
  - Maximum frequency of 933 MHz
  - ODT
  - Maximum capacity of 2 GB
  - Automatic power consumption control
- SPI NOR/NAND flash interface
  - 1-/2-/4-wire SPI NOR/NAND flash
  - Two CSs, connected to different types of flash memories
  - Maximum capacity of 64 MB for each CS (for the SPI NOR flash)
  - Maximum capacity of 512 MB for each CS (for the SPI NAND flash)

- 2 KB/4 KB page size (for the SPI NAND flash)
- 8-bit/1 KB or 24-bit/1 KB ECC (for the SPI NAND flash)
- Embedded 4 KB BOOTROM and 16 KB SRAM

RTC with an Independent Power Supply
- Independent battery for supplying power to the RTC

Configurable Boot Modes
- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash

SDK
- Linux 3.18-based SDK
- Audio encoding and decoding libraries complying with various protocols
- High-performance H.265/H.264 PC decoding library

Physical Specifications
- Power consumption
  - Typical power consumption of 2.5W
  - Multi-level power consumption control
- Operating voltages
  - 0.9 V core voltage
  - 1.0V CPU voltage
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Package
  - RoHS, TFBGA
  - Lead pitch of 0.8 mm (0.03 in.)
  - Body size of 19 mm x 19 mm (0.75 in. x 0.75 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)
The Hi3521D V100 is a professional SoC targeted for the multi-channel HD (1080p/720p) or SD (D1/960H) DVR. The Hi3521D V100 provides an ARM A7 dual-core processor, a high-performance H.265/H.264 video encoding/decoding engine, a high-performance video/graphics processing engine with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable the Hi3521D V100 to provide high-performance, high-picture-quality, and low-cost analog HD/SDI solutions for customers’ products while reducing the eBOM cost.

**DVRs (Each with a Hi3521D V100)**

**4x1080p DVR**
- 4x1080p@30 fps H.265 encoding+4xD1@30 fps H.265 encoding+4x1080p@30 fps H.265 decoding+4x1080p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

**8x720p DVR**
- 8x720p@30 fps H.265 encoding+8xD1@30 fps H.265 encoding+8x720p@30 fps H.265 decoding+8x720p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

**16x720p (Non-Real-Time)**
- 16x720p@15 fps H.265 encoding+16xD1@15 fps H.265 encoding+16x720p@15 fps H.265 decoding+16x720p@2 fps JPEG
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- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

16x960H DVR
- 16x960H@30 fps H.265 encoding +16xCIF@30 fps H.265 encoding +16x960H@30 fps H.265 decoding +16x960H@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs
## Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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<tbody>
<tr>
<td>3DES</td>
<td>triple data encryption standard</td>
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<tr>
<td>ADPCM</td>
<td>adaptive differential pulse code modulation</td>
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<td>AES</td>
<td>advanced encryption standard</td>
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<tr>
<td>CBR</td>
<td>constant bit rate</td>
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<tr>
<td>CS</td>
<td>chip select</td>
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<td>CVBS</td>
<td>composite video broadcast signal</td>
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<td>DCI</td>
<td>dynamic contrast improvement</td>
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<tr>
<td>DDR</td>
<td>double data rate</td>
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<tr>
<td>DES</td>
<td>data encryption standard</td>
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<td>DVR</td>
<td>digital video recorder</td>
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<td>eBOM</td>
<td>engineering bill of materials</td>
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<td>ECC</td>
<td>error correcting code</td>
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<td>eSATA</td>
<td>external serial advanced technology attachment</td>
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<td>GPIO</td>
<td>general-purpose input/output</td>
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<td>HD</td>
<td>high definition</td>
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<td>HDMI</td>
<td>high definition multimedia interface</td>
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<td>I²C</td>
<td>inter-integrated circuit</td>
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<td>I²S</td>
<td>inter-IC sound</td>
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<td>IR</td>
<td>infrared</td>
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<td>IVE</td>
<td>intelligent video engine</td>
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<td>MII</td>
<td>media independent interface</td>
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<td>ODT</td>
<td>on-die termination</td>
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<td>OSD</td>
<td>on-screen display</td>
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<td>PCM</td>
<td>pulse code modulation</td>
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<td>PM</td>
<td>port multiplexer</td>
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<td>QP</td>
<td>quantization parameter</td>
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<td>RGMII</td>
<td>reduced gigabit media independent interface</td>
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<tr>
<td>RMII</td>
<td>reduced media independent interface</td>
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<td>RoHS</td>
<td>Restriction of Hazardous Substances</td>
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<td>ROI</td>
<td>region of interest</td>
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<td>RTC</td>
<td>real-time clock</td>
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<td>SATA</td>
<td>serial advanced technology attachment</td>
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<tr>
<td>SD</td>
<td>standard definition</td>
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<tr>
<td>SDI</td>
<td>serial digital interface</td>
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<td>SDK</td>
<td>software development kit</td>
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<td>SDRAM</td>
<td>synchronous dynamic random access memory</td>
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<td>SoC</td>
<td>system-on-chip</td>
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<td>SPI</td>
<td>serial peripheral interface</td>
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<td>SRAM</td>
<td>static random access memory</td>
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<td>TDM</td>
<td>time division multiplexing</td>
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<td>TSO</td>
<td>TCP segmentation offload</td>
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<td>UART</td>
<td>universal asynchronous receiver transmitter</td>
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<td>VBR</td>
<td>variable bit rate</td>
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<td>VGA</td>
<td>video graphics array</td>
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<td>VI</td>
<td>video input</td>
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<td>VO</td>
<td>video output</td>
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