



Hi3798M V300 Brief Data Sheet

Key Specifications

High-Performance CPU

- Quad-core 64-bit high-performance ARM Cortex A53
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU

- Integrated high-performance multi-core GPU Mali-450
- OpenGL ES 2.0/1.1 and OpenVG 1.1

Memory Control Interfaces

- DDR3/DDR3L/DDR4 interface, supporting maximum 32-bit data width
- eMMC 5.0 flash interface
- Asynchronous/Synchronous NAND flash interface
 - SLC/MLC flash memory
 - Maximum 64-bit ECC

Video Decoding (HiVXE 2.0 Processing Engine)

- H.265/HEVC Main/Main 10 Profile@Level 5.1 high-tier, supporting 4K x 2K@60 fps decoding
- H.264/AVC Baseline Profile/Main Profile/High Profile@Level 5.1; H.264/AVC MVC, supporting 4K x 2K@30 fps decoding
- VP9 10-bit, supporting 1080p@60 fps decoding
- 1080p@60 fps decoding, supported by MPEG-1
- MPEG-2 Simple Profile@Main Level, Main Profile@High Level, supporting 1080p@60 fps decoding
- MPEG-4 Simple Profile@Levels 0–3, ASP@Levels 0–5, supporting GMC, short header format, and 1080p@60 fps decoding
- AVS-P16 (AVS+), supporting 1080p@60 fps decoding

Image Decoding

- JPEG decoding, maximum 64 megapixels
- PNG decoding, maximum 64 megapixels

Video and Image Encoding

- H.265 MP@level 5 main tier and H.264 BP/MP/HP@level 4.2 video encoding, maximum 1x1080p@30 fps
- VBR or CBR mode for video encoding
- Low-delay encoding
- Multi-ROI encoding

Audio Encoding and Decoding

- MPEG L1/L2
- Dolby Digital/Dolby Digital Plus decoder-converter
- Dolby Digital/DTS passthrough
- Dolby Atmos
- AAC-LC and HE-AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- G.711 (u/a) audio decoding
- G.711 (u/a), AMR-NB, AMR-WB, and AAC-LC audio encoding
- HE-AAC transcoding DD (AC3)

Security Processing

- Secure boot, secure storage, and secure upgrade
- ChinaDRM
- HDCP 2.2/1.4 for HDMI outputs

Graphics and Display Processing (Imprex 2.0 Processing Engine)

- HDR10/HLG HDR/SLF HDR

- Image enhancement algorithm
- Conversion from HDR to SDR
- Hardware overlaying of multi-channel graphics and video inputs
- Multiple graphics layers and video layers
- Multi-order vertical and horizontal scaling of videos and graphics; free scaling
- Screen mirroring and video rotation
- Full-format 3D video processing and display
- Enhanced TDE
- Anti-aliasing, anti-flicker, enhancement of image colors and luminance, NR, DEI, sharpening, as well as adjustment of the luminance, chrominance, contrast, and saturation
- Ultra-low-delay video processing

Audio and Video Interfaces

- PAL or NTSC standard output and forcible standard conversion
- Aspect ratio of 4:3 or 16:9, forcible aspect ratio conversion, and free scaling
- 4K@60 fps/50 fps/30 fps/25 fps, 1080p@60 fps/50 fps/30 fps/24 fps, 1080i@60 fps/50 fps, and 720p/576p/576i/480p/480i outputs
- HD and SD outputs
- One HDMI 2.0b TX with HDCP 2.2 output, supporting maximum 4K x 2K@60 fps resolution
- Analog video interfaces
 - One CVBS interface
 - One internal VDAC
- Audio interface
 - Audio-left and audio-right outputs
 - One internal ADAC
 - One I²S or PCM digital audio input or output
 - HDMI audio output

Peripheral Interfaces

- Three USB 2.0 host ports
- One 10 Mbit/s or 100 Mbit/s adaptive Ethernet port (embedded FE PHY)
- One 4-bit SDIO 3.0 interface
- Three UART interfaces
- One IR receiver
- One LED and keypad control interface
- Three I²C interfaces
- Multiple groups of GPIO interfaces
- One embedded POR

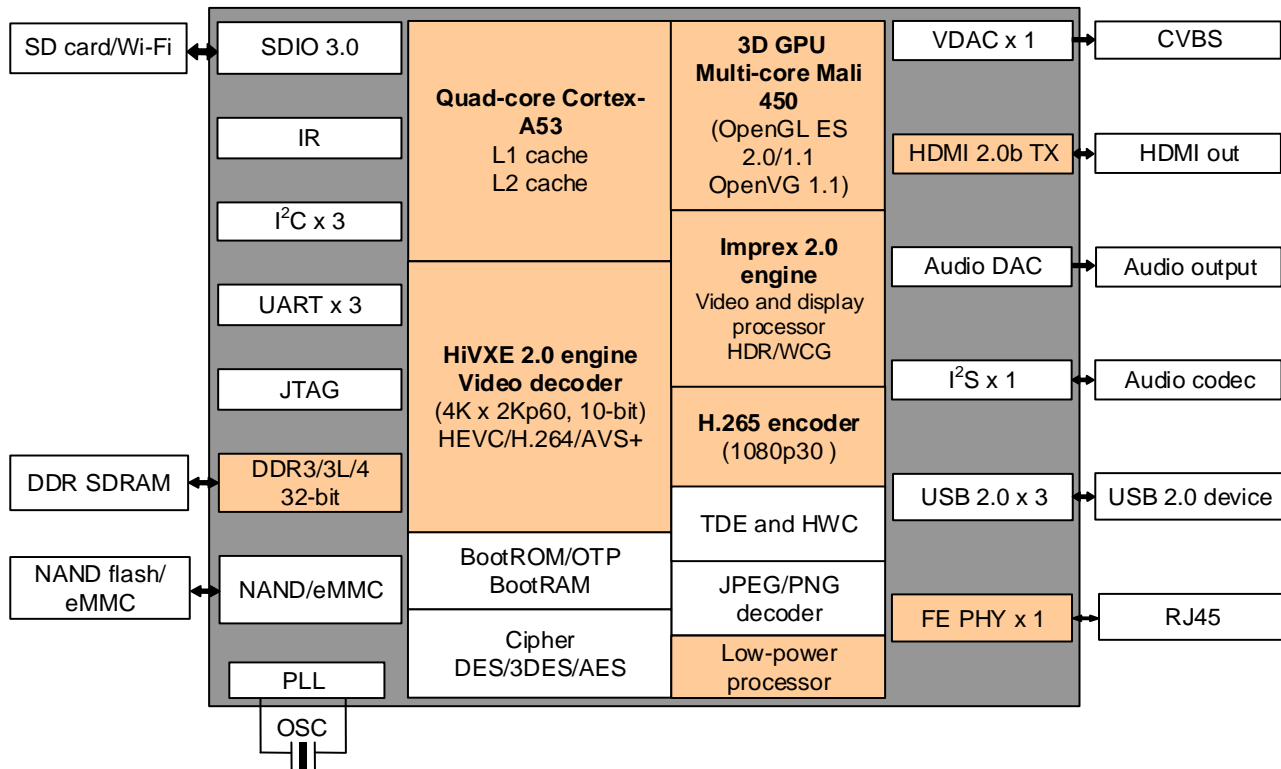
Others

- Various boot modes
- Boot program downloading and execution over a serial port or USB port
- Integrated dedicated standby processor, supporting various low-power modes and less than 30 mW standby power consumption
- Passive standby and low-power design
- 14 mm x 14 mm (0.55 in. x 0.55 in.) BGA package, supporting the 2-layer PCB



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Functional Block Diagram



Hi3798M V300 is a full-4K high-performance SoC that supports 4Kp60 decoding and is targeted for the IPTV/OTT STB market. Hi3798M V300 integrates the 4-core 64-bit high-performance Cortex-A53 processor and multi-core high-performance 2D/3D acceleration engine. Hi3798M V300 supports H.265 4K x 2K@P60 10-bit UHD video decoding, high-performance H.264 HD video encoding, HDR video decoding and display, and Dolby and DTS audio processing. Hi3798M V300 also provides various peripheral interfaces such as USB 2.0 and SDIO 3.0 interfaces. These features help customers implement full-4K service deployment and enable Hi3798M V300 to provide the best user experience in the industry in aspects of picture quality, stream compatibility, video playing smoothness, and STB performance, meeting the requirements of continuously increasing value-added services such as video communication, karaoke, cloud gaming, and multi-screen interaction.

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Acronyms and Abbreviations

AAC-LC	Advanced Audio Coding Low Complexity
ADAC	audio digital-to-analog converter
AMR-NB	adaptive multi-rate narrowband
AMR-WB	adaptive multi-rate wideband
APE	Monkey's Audio
ASP	audio signal processing
AVC	Advanced Video Coding
AVS	Audio Video Standard
BGA	ball grid array
CBR	constant bit rate
CPU	central processing unit
CVBS	Composite Video Broadcast Signal
DD	Dolby Digital
DDR	double data rate
DEI	deinterlacing
DRM	digital rights management
DTS	Digital Theater Systems
ECC	error checking and correction
eMMC	embedded multimedia card
ES	elementary stream
FE	fast Ethernet
FLAC	Free Lossless Audio Codec
GMC	global motion compensation
GPIO	general-purpose input/output
GPU	graphics processing unit
HD	high definition
HDCP	High-bandwidth Digital Content Protection
HDMI	high definition multimedia interface
HDR	high dynamic range
HE-AAC	High-Efficiency Advanced Audio Coding
HEVC	High Efficiency Video Coding
HLG	Hybrid Log-Gamma
I ² C	inter-integrated circuit
IR	infrared
I ² S	inter-IC sound
IPTV	Internet Protocol television
JPEG	Joint Photographic Experts Group
MLC	multi-level cell
MPEG	Moving Picture Experts Group
MVC	multiview video coding
NR	noise reduction
NTSC	National Television System Committee
OTT	over-the-top
PAL	Phase Alternating Line
PCB	printed circuit board
PCM	pulse-code modulation
PHY	Port Physical Layer
PNG	Portable Network Graphics
POR	power-on reset
ROI	region of interest
SD	standard definition
SDIO	Secure Digital Input Output
SDR	standard dynamic range



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SLC	single-level cell
SLF	scene luminance fidelity
SoC	system on chip
STB	set-top box
TDE	two-dimensional engine
TX	transmit
UART	universal asynchronous receiver transmitter
UHD	ultra high definition
VBR	variable bit rate
VDAC	video digital-to-analog converter