



Hi3556A V100 Ultra-HD Mobile Camera SoC

Brief Data Sheet

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Hi3556A V100 Ultra-HD Mobile Camera SoC

Introduction

Hi3556A V100 is a high-performance and low-power 4K ultra-HD mobile camera SoC designed for mobile cameras, panoramic cameras, rear view mirrors, and unmanned aerial vehicles (UAVs). It supports the H.265 and H.264 encoding and decoding with performance up to 4K x 2K@60 fps and 1080p@240 fps. Integrating with the HiSilicon fourth-generation image sensor processor (ISP), Hi3556A V100 supports wide dynamic range (WDR), multi-level noise reduction (NR), Six degrees of freedom (6DoF) digital image stabilization (DIS), and ample algorithms for image enhancement and correction, delivering professional image quality. Hi3556A V100 also supports 4K raw data output, facilitating post editing. With the advanced low-power process and architecture design, Hi3556A V100 provides users with long-lasting battery life.

Hi3556A V100 supports multiple sensor inputs and built-in high-performance any view stitching (AVS) engine to implement 4K 2-channel to 4-channel real-time panoramic video stitching.

With the hardware-based 6DoF DIS, Hi3556A V100 has reduced its dependence on the mechanical head during 4K@60 fps video recording.

Hi3556A V100 provides efficient and ample computing resources to assist customers in developing consumer applications and industry applications. Hi3556A V100 integrates a dual-core A53 processor and one digital signal processor (DSP) and offers the dual-system solution, enabling fast startup, real-time performance, and connections with rich peripheral drives.

Hi3556A V100 supports the product miniaturization design because it uses the advanced 12 nm low-power process and miniaturization package and supports DDR4/LPDDR4/LPDDR3 SDRAMs.

With the stable and easy-to-use mobile SDK design provided by HiSilicon, Hi3556A V100 can assist customers in rapid product mass production.

Key Features

- **Low Power Consumption**
 - 1.7 W power consumption in a typical scenario for 4K x 2K (3840 x 2160)@60 fps H.265 encoding
- **4K@60 fps Encoding**
 - 4K x 2K (3840 x 2160)@60 fps or 1080p@240 fps H.265/H.264 encoding.
- **Multi-Sensor Inputs**
 - Up to 5-sensor inputs, supporting panoramic cameras and UAVs
- **Hardware-based Multi-Channel Video Stitching**
 - 2-channel 3K x 3K (3000 x 3000)@30 fps or 4-channel 1080p@30 fps stitching and recording
- **High-Performance Intelligent Analysis**
 - Multiple functions such as face detection and recognition, target detection and tracking, and high-level API invoking through underlying hardware. Easy combination with photographing/video recording to implement various personalized and creative applications
 - Integrated high-performance DSP facilitating developing customer algorithms and implementing product differentiation
- **High-Speed Memory Interfaces**
 - USB 3.0 high-speed interface



Hi3556A V100 Ultra-HD Mobile Camera SoC

Key Specifications

Processor Core

- Dual-core ARM Cortex A53@1.2 GHz, 32 KB I cache, 32 KB D cache or 256 KB L2 cache
- Neon acceleration and integrated FPU
- Linux+Huawei LiteOS dual-system solution

DSP

- Integrated Tensilica Vision P6 DSP@630 MHz
- 32 KB I cache, 32 KB I RAM, 512 KB data RAM
- Huawei LiteOS

Video Codec

- H.265 main profile, L5.1
- H.264 baseline/main/high profile, L5.1
- I-/P-/B-slice supported in H.264/H.265 codec
- JPEG baseline codec
- Maximum resolution for H.264/H.265 codec: 8192 x 8192
- H.265/H.264 codec performance:
 - 3840 x 2160@60 fps + 720p@30 fps encoding
 - 3840 x 2160@60 fps decoding
 - 3840 x 2160@30 fps encoding + 3840 x 2160@30 fps decoding
- Maximum resolution for JPEG encoding: 8192 x 8192
- JPEG codec performance: 16MP (4608 x 3456)@30 fps
- CBR, VBR, and FixQp bit rate control modes
- Maximum bit rates for H.265 and H.264 encoding outputs respectively: 120 Mbit/s and 200 Mbit/s
- Encoding of eight ROIs

Video input interface

- 12-lane image sensor serial inputs, and MIPI, sub-LVDS, HiSPi, and SLVS-EC interfaces.
- Up to 5-sensor serial inputs and multiple combination modes: 12-lane, 8-lane+4-lane, or 4-lane+4 x 2-lane
- Maximum input resolution: 7680 x 4320
- 10-/12-/14-bit Bayer RGB DC timing VI
- BT.656 and BT.1120 VI
1-channel to 4-channel YUV inputs through the MIPI virtual channels

ISP and Image Processing

- Multi-channel TDM to process multi-sensor video inputs.
- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- 2-frame WDR exposure, local tone mapping, strong light suppression, and backlight compensation
- Defect pixel correction and lens shading correction
- Multi-level 3DNR, which removes motion smearing and chroma noise and provides excellent image effects in low illumination
- 3D-LUT color adjustment
- Image dynamic contrast enhancement and edge enhancement
- CAC and purple fringe removal
- Dehaze

- 6DoF DIS and rolling shutter correction
- Lens GDC and fisheye correction
- Picture rotation by 90° or 270°
- Image mirroring and flipping
- Multi-channel 1/15.5x–16x scaling outputs
- OSD overlaying of up to eight regions before encoding
- ISP adjustment tool on the PC

2D Graphics Processing

- BitBlt operation
- Line drawing
- Alpha blending
- Color key
- CSC

Hardware Accelerated Engine for Video Stitching

- 2-channel and 4-channel AVS
- Stitching performance:
 - 2-channel 3000 x 3000@30 fps VI and 3840 x 2160@30 fps VO
 - 4-channel 1080 x 1920@30 fps VI and 3840 x 2160@30 fps VO

VO Interface

- HDMI 2.0, supporting up to 4K x 2K (4096 x 2160)@60 fps VO
- 4-lane MIPI DSI, supporting up to 1080p@60 fps VO
- 6-/8-/16-/24-bit digital LCD/BT.656/BT.1120 interface, supporting up to 1080p@60 fps RGB/YUV VO
- HDMI+non-homologous LCD

Intelligent Analysis

- Hardware acceleration for face detection
- Hardware acceleration for target detection
- Hardware acceleration for binocular depth map computing with processing performance of 720p@30 fps
- Hardware acceleration for IVE 2.1 intelligent operators for feature point detection, optical flow, and computer morphology processing, and so on

Audio Interface

- Integrated audio codec, supporting 16-bit audio inputs and outputs
- Dual-channel differential MIC inputs for reducing background noises
- I²S interface for 8-channel audio TDM inputs and dual-channel audio outputs (mutually exclusive with the built-in audio codec).
- HDMI audio outputs

Audio Encoding and Decoding

- Voice codec complying with multiple protocols by software
- Audio encoding in formats such as G.711, G.726, and AAC
- Audio VQE processing



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Security Engine

- AES, DES, and 3DES encryption and decryption algorithms implemented by hardware
- RSA1024/2048/3072/4096 signature verification algorithm implemented by using hardware
- HASH-SHA1/224/256/384/512 and HMAC_SHA1/224/256/384/512 tamper proofing algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and hardware random number generator
- Secure boot

Peripheral Interface

- Two SDIO 3.0 interfaces:
 - SDIO 0 supports the SDXC card.
 - SDIO 1 supports the Wi-Fi module.
- One USB 3.0 port and one USB 2.0 port, with configurable host or device mode
- Internal POR signal output and external reset input.
- Independent battery for the built-in RTC
- Integrated 4-channel LSADC
- Nine UART interfaces (Some pins are multiplexed with other pins.)
- Multiple I²C interfaces, SPIs, and GPIO interfaces
- One IR interface
- Eight PWM interfaces (Some pins are multiplexed with other pins.)

External Memory Interface

- 32-bit DDR4/LPDDR4/LPDDR3 SDRAM interface
 - Maximum clock frequency of 1333 MHz for the DDR4/LPDDR4 SDRAM
 - Maximum clock frequency of 933 MHz for the LPDDR3 SDRAM
 - Maximum DDR address space of 3.5 GB
- SPI NOR flash interface
 - 1-/2-/4-line mode
 - 3-/4-byte address modes.
 - Maximum capacity of 256 MB
- SPI NAND flash interface
 - SLC flash
 - 2 KB/4 KB page size
 - 8-/24-/28-bit ECC (unit: 1 KB)
 - Maximum capacity of 1 GB
- NAND flash interface
 - 8-bit data width
 - SLC flash
 - 2 KB/4 KB page size
 - 8-/16-/24-bit ECC (ECC unit: 1 KB)
 - Maximum capacity of 1 GB
- eMMC 5.1 interface
 - HS400
 - Maximum capacity of 2 TB

Configurable Boot Mode

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash
- Booting from the NAND flash
- Booting from the eMMC

Image Burning Mode

- Image burning through UART 0
- Image burning through an SD card
- Image burning through a USB device

SDK

- Linux+Huawei LiteOS dual-system solution
- High-performance H.265 decoding library for iOS and Android

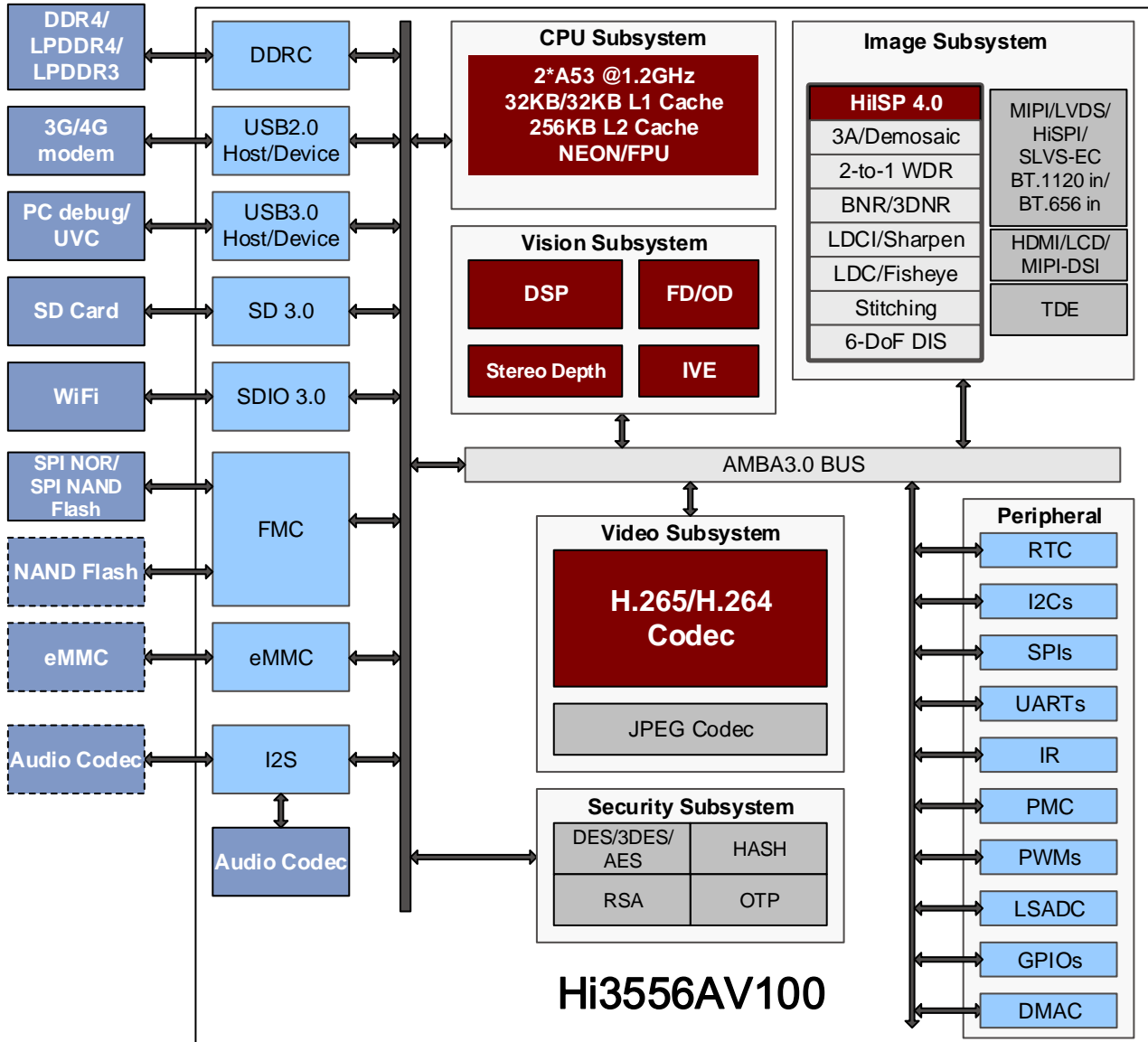
Physical Specifications

- Power consumption
 - 1.7 W power consumption in a typical scenario for 4K x 2K (3840 x 2160)@60 fps encoding
 - Multi-level power saving mode
- Operating voltage
 - 0.8 V core voltage
 - 1.8 V or 3.3 V I/O voltage
 - 1.2 V LPDDR3/DDR4 SDRAM interface voltage
 - 1.1 V LPDDR4 SDRAM interface voltage
- Package
 - RoHS, FCCSP
 - Body size: 15 mm x 15 mm x 1.0 mm (0.59 in. x 0.59 in. x 0.04 in.)
 - Lead pitch: 0.65 mm and 0.4 mm hybrid pitch
 - Operating temperature range: 0–70°C (32°F–158°F)



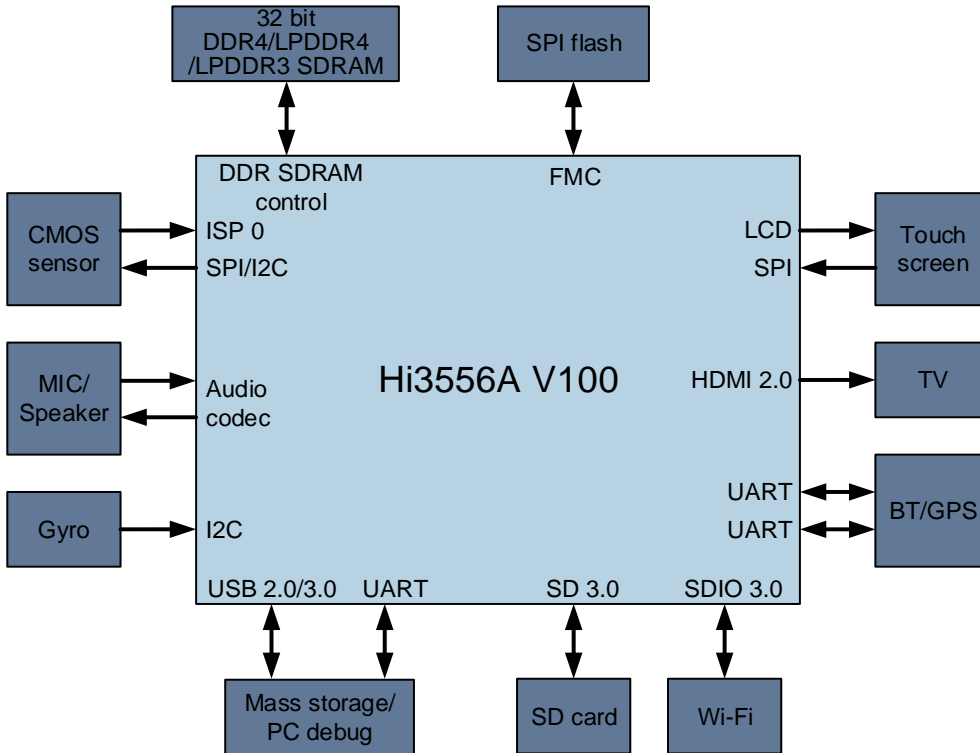
Hi3556A V100 Ultra-HD Mobile Camera SoC

Functional Block Diagram



Hi3556A V100 Ultra-HD Mobile Camera SoC

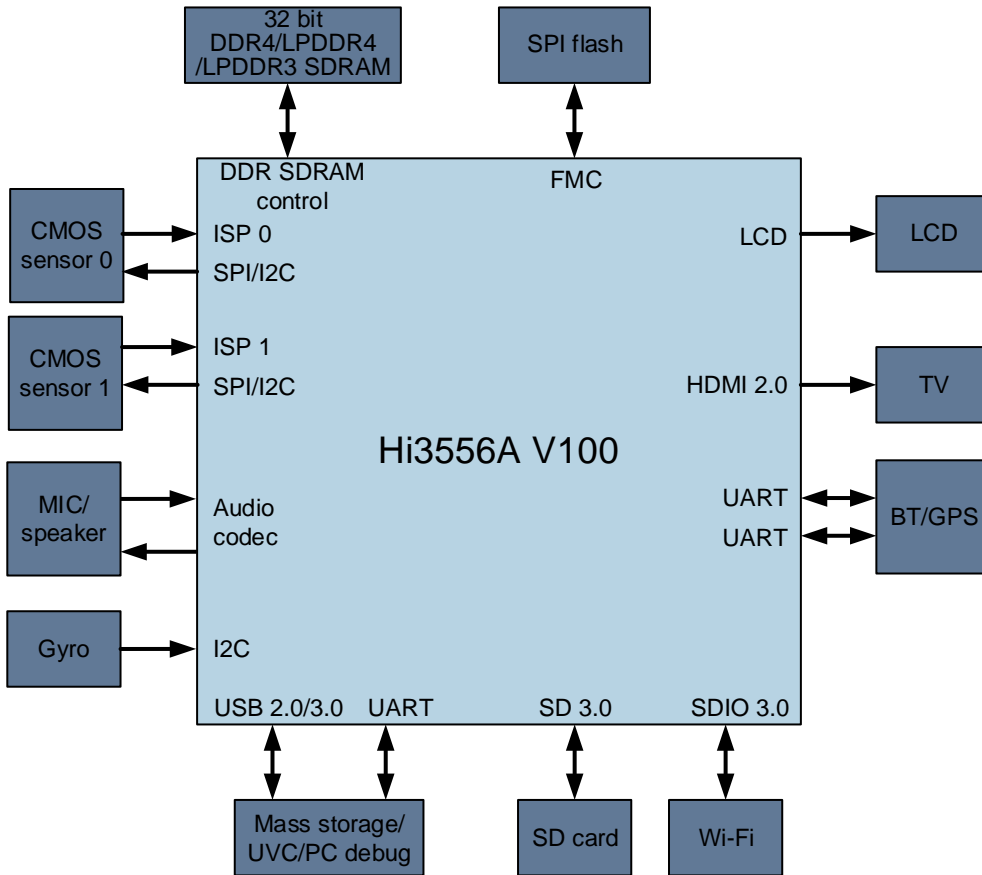
Hi3556A V100 Mobile Camera Solution



- Video recording mode: 4K x 2K (3840 x 2160)@60 fps for SD card storage+1080p@30 fps sub stream encoding for Wi-Fi VOD and preview
- 4K x 2K (3840 x 2160)@60 fps 6DoF DIS and 3-axis Gyro OIS
- Photographing mode: 16MP@30 fps continuous shooting
- Playback mode: 4K x 2K (3840 x 2160)@60 fps decoding+HDMI 4K x 2K (3840 x 2160)@60 fps for TV display+independent LCD
- Two 16-bit DDR4 SDRAMs (2666 Gbit/s) or one 32-bit LPDDR4 SDRAM (2666 Gbit/s)
- Dual MICs and advanced dual-MIC NR algorithm

Hi3556A V100 Ultra-HD Mobile Camera SoC

Hi3556A V100 Panoramic Camera Solution

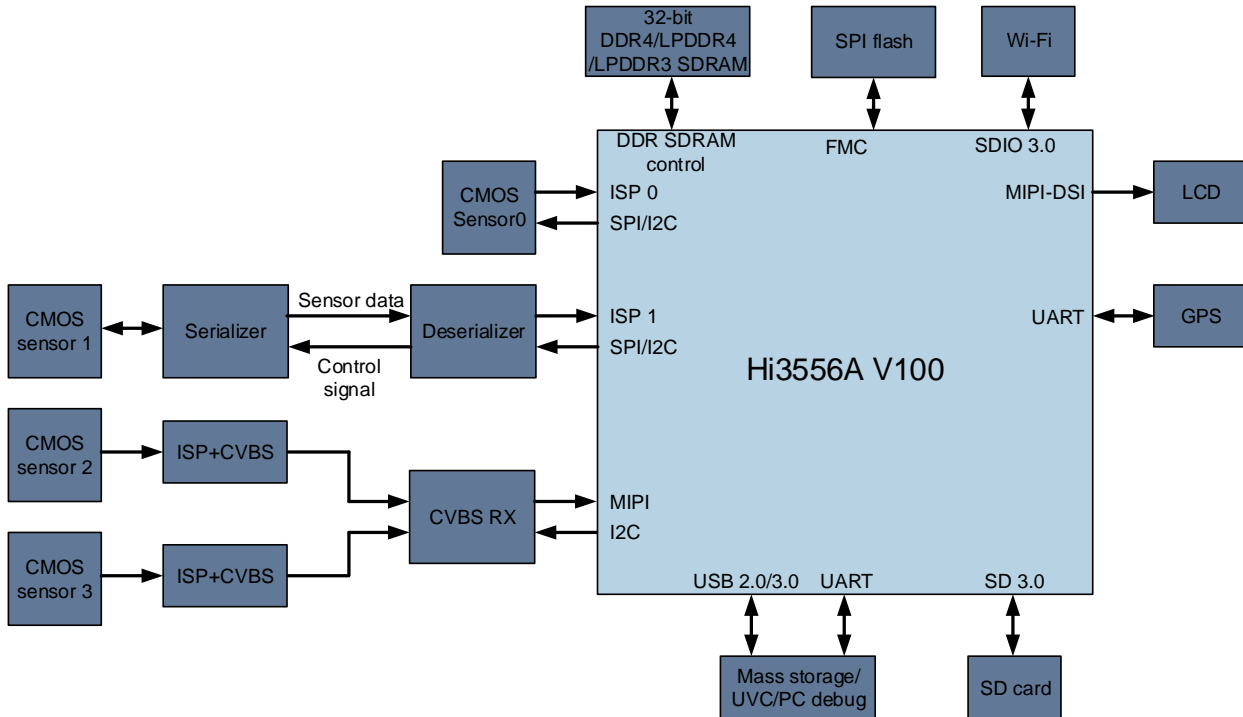


- 2-channel 3K x 3K (3000 x 3000)@30 fps inputs or 4-channel 1K x 2K (1080 x 1920) inputs, 4K x 2K (3840 x 2160)@30 fps after stitching, 4K x 2K (3840 x 2160)@30 fps encoding for SD card storage, and 1080p@30 fps sub streams of longitudes and latitudes for Wi-Fi TX and VOD
- Two 16-bit DDR4 SDRAMs (2666 Gbit/s) or one 32-bit LPDDR4 SDRAM (2666 Gbit/s)
- Two SDIO 3.0 interfaces, extended low-power Wi-Fi module, and external SDXC card
- Dual MICs or four MICs (external ADC required). The CPU and DSP are used for complex 3D audio recording algorithm.



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Hi3556A V100 Vehicle-Mounted Multi-Camera Solution



- Video data (Bayer RGB format) captured by one to four sensors over the MIPI (Long-distance transmission of sensor data can be implemented through the SerDes link)
- Dual-channel 4MP (2560 x 1440)@30 fps H.265 encoding
- One to four channels 1080p@30 fps composite (YUV422 format) VI over the MIPI, which can be used to implement 360° view
- MIPI-DSI interface for the 1080p curved screen and low-delay preview
- DSP and intelligent hardware accelerated engine for implementing the ADAS algorithm.
- Two 16-bit DDR4 SDRAMs (2666 Gbit/s) or one 32-bit LPDDR4 SDRAM (2666 Gbit/s)



Acronyms and Abbreviations

3DES	triple data encryption standard
3DNR	three-dimensional noise reduction
6DoF	six degrees of freedom
AAC	advanced audio coding
ADC	analog to digital converter
AE	automatic exposure
AES	advanced encryption standard
AF	automatic focus
API	application programming interface
AVS	any view stitching
AWB	automatic white balance
CAC	chromatic aberration correction
CBR	constant bit rate
CMOS	complementary metal-oxide-semiconductor
codec	coder/decoder
DC	digital camera
DDR	double data rate
DES	data encryption standard
DIS	digital image stabilization
DoF	degree of freedom
DPC	defect pixel correction
DSP	digital signal processor
ECC	error-correcting code
EDR	event data recorder
eMMC	embedded multimedia card
FCCSP	flip-chip chip scale package
FPN	fixed pattern noise
FPU	floating-point unit
GDC	geometric distortion correction
GPIO	general-purpose input/output
GPU	graphics processing unit
HD	high definition
HDMI	high definition multimedia interface
HiSPi	high-speed serial pixel interface
I2C	inter-integrated circuit
IR	infrared
ISP	image signal processor
IVE	intelligent video engine
LCD	liquid crystal display
LPDDR	low-power double data rate
LSADC	low-speed analog-to-digital converter
LUT	lookup table
LVDS	low-voltage differential signaling
MCU	microcontroller unit
MIC	microphone
MIPI	mobile industry processor interface
MPP	media processing platform
NR	noise reduction
OIS	optical image stabilization
OS	operating system
OSD	on-screen display

**Hi3556A V100 Ultra-HD Mobile Camera SoC**

OTP	one-time programming
POR	power-on reset
PWM	pulse-width modulation
PWM	pulse-width modulation
RC	root complex
RGB	red-green-blue
RoHS	Restriction of hazardous substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SD	secure digital
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SDXC	secure digital extended capacity
SLC	single-level cell
SLVS-EC	Scalable Low Voltage Signaling interface with Embedded Clock
SoC	system-on-chip
SPI	serial peripheral interface
SVP	Smart Vision Process
TDM	time division multiplexing
TX	transmit
UART	universal asynchronous receiver transmitter
UAV	unmanned aerial vehicle
USB	Universal Serial Bus
VBR	variable bit rate
VI	video input
VO	video output
VOD	video on demand
VQE	voice quality enhancement
WDR	wide dynamic range