Hi3518E V300 Consumer Camera SoC

Major Specifications

Processor Core
- ARM Cortex-A7@ 900 MHz, 32KB I-Cache, 32KB D-Cache /128KB L2 cache
- NEON acceleration and the integrated floating-point processing unit (FPU)

Video Encoding
- H.264 BP/MP/HP, supporting I-/P- frames
- H.265 MP, supporting I-/P- frames
- MJPEG/JPEG baseline encoding

Video Encoding Performance
- Maximum resolution for H.264 /H.265 encoding: 2304 x 1296 (with the width up to 2304)
- Real-time multi-stream H.264/H.265 encoding capability:
  - 2048 x 1536@20 fps + 720x576@20 fps
  - 2304 x 1296@20 fps + 720x576@20 fps
  - 1920 x 1080@30 fps + 720x576@30 fps
- JPEG snapshot at 3M (2304 x 1296)@5 fps
- CBR, VBR, FIXQP, AVBR, QPMAP and CVBR bit rate control modes
- Intelligent encoding mode
- Up to 60 Mbit/s output bit rate
- Encoding of eight ROIs

Intelligent Video Analysis
- Integrated IVE, supporting human detection for intelligent applications such as facial and abnormal sound detection
- Various intelligent analysis applications, such as intelligent motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing
- 3DNR, image enhancement, and DCI
- Anti-flicker for output videos and graphics
- 1/15x to 16x video and graphics scaling
- Overlaying of videos and graphics
- Image rotation by 90°, 180°, or 270°
- Image mirror and flip
- OSD overlaying of eight regions before encoding

ISP
- 4 x 4 pattern RGB-IR sensor
- 3A (AE, AF, and AWB) function. The third-party 3A algorithms are supported.
- FPN removal and DPC
- LSC, LDC, and purple edge correction
- Direction-adaptive demosaic
- Gamma correction, DCI, and color management and enhancement
- Adaptive region de-fog
- Multi-level NR (BayerNR and 3DNR) and sharpening enhancement
- Local tone mapping
- Sensor built-in WDR
- 2F-WDR frame-based mode
- DIS
- Intelligent ISP tuning and ISP tuning tools for the PC

Audio Encoding and Decoding
- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726, and ADPCM protocols
- Audio 3A functions (AEC, ANR, and AGC)

Security Engine
- AES/RSA encryption and decryption algorithms implemented by using hardware
- HASH (SHA1/SHA256/ HMAC_SHA1/HMAC_SHA256) algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and random number generator

Video Interfaces
- Input
  - 8-/10-/12-bit RGB Bayer DC timing VI
  - MIPI, LVDS/sub-LVDS, and HiSPI
  - Compatibility with mainstream HD CMOS sensors provided by Sony, ON, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
  - Maximum input resolution: 2304 x 1296
- Output
  - 6-/8-bit LCD output
  - BT.656/BT.1120 output

Audio Interfaces
- Integrated audio codec, supporting 16-bit audio input and output
- Dual MIC/line-in input
- Mono line-out output
- I²S interface for connecting to external audio codec

Peripheral Interfaces
- POR
- Integrated high-precision RTC
- Integrated 2-channel LSADC
- Three UART interfaces
- I²C, SPI, and GPIO interfaces
- Four PWM interfaces
- One SDIO 2.0 interface and one SD 2.0 card interface
- One USB 2.0 host/device port
- PMC standby control unit

External Memory Interfaces
- SDRAM interface
  - Built-in 512 Mb DDR2

Hi3518E V300 Consumer Camera SoC

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- SPI NOR flash interface
  - 1-/2-/4-line mode
  - Maximum capacity: 256 MB
- SPI NAND flash interface
  - 1-/2-/4-line mode
  - Maximum capacity: 1 GB
- eMMC 4.5 interface
  - 4-bit data width

**Boot**
- Booting from the SPI NOR flash memory, SPI NAND flash memory, or eMMC
- Secure boot

**SDK**
- Huawei LiteOS/Linux-4.9-based SDK
- High-performance H.264 PC decoding library
- High-performance H.265 PC, Android, and iOS decoding libraries

**Physical Specifications**
- Power consumption
  - Typical power consumption in the 1080P30/3M20 scenario: 700 mW
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V I/O voltage (±10%)
  - 1.8 V SDRAM interface voltage
- Packaging
  - 9 mm x 9 mm, 88 pins, 0.35 mm ball pitch, QFN package

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Hi3518E V300 is a new-generation SoC designed for consumer cameras. It introduces a new-generation ISP and the latest H.265 video encoder. It supports human detection, providing intelligent applications such as facial and abnormal sound detection. It uses the advanced low-power technology and architecture design. All of these features enable Hi3518E V300 to lead the industry in the low bit rate, high picture quality, and low power consumption. It also integrates with the POR, RTC, and audio codec, greatly reducing the EBOM cost for customers.
Hi3518E V300 Consumer Camera Solution

Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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<tbody>
<tr>
<td>3DNR</td>
<td>three-dimensional noise reduction</td>
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<tr>
<td>BP</td>
<td>Baseline Profile</td>
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<tr>
<td>AE</td>
<td>automatic exposure</td>
</tr>
<tr>
<td>AES</td>
<td>advanced encryption standard</td>
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<tr>
<td>AF</td>
<td>auto focus</td>
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<tr>
<td>AWB</td>
<td>automatic white balance</td>
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<tr>
<td>CBR</td>
<td>constant bit rate</td>
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<tr>
<td>DDR</td>
<td>double data rate</td>
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<tr>
<td>DES</td>
<td>data encryption standard</td>
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<tr>
<td>DIS</td>
<td>digital image stabilization</td>
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<tr>
<td>EBOM</td>
<td>engineering bill of materials</td>
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<tr>
<td>HDMI</td>
<td>high definition multimedia interface</td>
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<td>HiSPI</td>
<td>high-speed serial pixel interface</td>
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<tr>
<td>HP</td>
<td>High Profile</td>
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<tr>
<td>IR</td>
<td>infrared spectrum</td>
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<tr>
<td>ISP</td>
<td>image signal processor</td>
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<tr>
<td>IVE</td>
<td>intelligent video engine</td>
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<tr>
<td>LSADC</td>
<td>low-speed analog-to-digital converter</td>
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<td>LSC</td>
<td>lens shading correction</td>
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<td>LVDS</td>
<td>low-voltage differential signaling</td>
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<tr>
<td>MIC</td>
<td>microphone</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
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<tr>
<td>MIPI</td>
<td>mobile industry processor interface</td>
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<tr>
<td>MP</td>
<td>Main Profile</td>
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<tr>
<td>NR</td>
<td>noise reduction</td>
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<tr>
<td>OSD</td>
<td>on-screen display</td>
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<tr>
<td>OTP</td>
<td>one-time programmable</td>
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<td>POR</td>
<td>power-on reset</td>
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<tr>
<td>PWM</td>
<td>pulse-width modulation</td>
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<tr>
<td>QFN</td>
<td>Quad Flat No-lead Package</td>
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<tr>
<td>ROI</td>
<td>region of interest</td>
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<tr>
<td>RSA</td>
<td>Rivest-Shamir-Adleman</td>
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<tr>
<td>RTC</td>
<td>real-time clock</td>
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<tr>
<td>SDIO</td>
<td>secure digital input output</td>
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<tr>
<td>SDK</td>
<td>software development kit</td>
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<tr>
<td>SDRAM</td>
<td>synchronous dynamic random access memory</td>
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<tr>
<td>SoC</td>
<td>system on a chip</td>
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<tr>
<td>UART</td>
<td>universal asynchronous receiver transmitter</td>
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<tr>
<td>VBR</td>
<td>variable bit rate</td>
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<tr>
<td>VI</td>
<td>video input</td>
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<tr>
<td>VO</td>
<td>video output</td>
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<td>WDR</td>
<td>wide dynamic range</td>
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