Hi3559C V100 ultra-HD Mobile Camera SoC

Brief Data Sheet

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Introduction

Hi3559C V100 is a professional 8K ultra-HD mobile camera SoC. It supports 8K30/4K120 digital video recording with broadcast quality. It also supports multiple sensor inputs as well as the H.265 encoding output or movie-level raw data output. It integrates the high-performance ISP and employs the advanced low-power process and architecture design. Hi3559C V100 provides excellent image processing capability.

Hi3559C V100 supports the industry-leading multi-channel 4K sensor inputs, multi-channel ISP image processing, HDR10 technology standard, and multi-channel panoramic hardware stitching. With the 6-DOF DIS hardware, Hi3559C V100 has reduced its dependence on the mechanical head during 8K30/4K120 video recording.

Hi3559C V100 provides efficient and ample computing resources to assist customers in developing consumer applications and industry applications. Hi3559C V100 integrates the dual-core A73 processor and dual-core A53 processor as well as the big.LITTLE architecture and dual operating systems, achieving balance between the power consumption and startup time.

Hi3559C V100 supports the product miniaturization design because it uses the advanced 12 nm low-power process and miniaturization package and supports DDR4/LPDDR4 SDRAMs.

With the stable and easy-to-use mobile SDK design provided by HiSilicon, Hi3559C V100 can assist customers in rapid product mass production.

Key Features

- **Low Power Consumption**
  Typical power consumption of 3 W in 8K30 (7680 x 4320)+1080p30 H.265 encoding mode

- **Package**
  15 mm x 15 mm (0.59 in. x 0.59 in.) FC-CSP

- **8K30/4K120 Encoding**
  8K30+1080p30 or 4K120+1080p30 H.265 encoding

- **Multi-Channel Video Recording**
  2x4K60, 4x4K30, or 8x1080p30 video recording, supporting hardware stitching within the camera

- **High-Speed Memory Interfaces**
  USB 3.0 or PCIe 2.0 high-speed interface
  UFS and eMMC interfaces

- **Raw Video Output**
  Professional 4K30 raw video output

- **Visual Computing Processing Capability**
Key Specifications

Processor Core
- Dual-core ARM Cortex A73@1.8 GHz, 32 KB I cache, 64 KB D cache or 512 KB L2 cache
- Dual-core ARM Cortex A53@1.2 GHz, 32 KB I cache, 32 KB D cache or 256 KB L2 cache
- Single-core ARM Cortex A53@1 GHz, 32 KB I cache, 32 KB D cache or 128 KB L2 cache
- Neon acceleration and integrated FPU

GPU
- Dual-core ARM Mali G71@900 MHz, 256 KB cache
- OpenCL 1.1/1.2/2.0
- OpenGL ES 3.0/3.1/3.2

Sensor Hub
- Integrated ARM Cortex M7@192 MHz
- Integrated PMC, which supports only external reset
- Internal POR
- General peripheral IPs (UART, SPI, I²C, PWM, GPIO, and LSADC)
- 2-channel LSADC, seven UART interfaces, and eight PWM interfaces

Video Encoding
- H.264 BP/MP/HP
- H.265 Main Profile/Main 10 Profile
- I/P/B frame supported in H.264/H.265 encoding mode
- MJPEG/JPEG Baseline encoding
- A maximum of 8192 x 8640 resolution for H.264 encoding
- A maximum of 16384 x 8640 resolution for H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capability:
  - 7680 x 4320@30 fps+1080p@30 fps+7680 x 4320@2 fps snapshot
- Maximum MJPEG snapshot performance of 7680 x 4320@15 fps
- CBR, VBR, AVBR, FIXQP, and QPMAF bit rate control modes
- Maximum 200 Mbit/s output bit rate
- Encoding of eight ROIs

Video Decoding
- H.264 BP/MP/HP
- H.265 Main Profile/Main 10 Profile
- JPEG/MJPEG decoding
- Maximum video decoding performance of H.264/H.265
  7680 x 4320@30 fps or H.264/H.265 3840 x 2160@120 fps
- Maximum 7680 x 4320@15 fps JPEG decoding

Intelligent Video Processing
- Visual computing processing capability
- Quad-core DSP@700 MHz, 32 KB I cache, 32 KB IRAM, or 512 KB DRAM
- Dual-core NNIE@840 MHz neural network acceleration
- Internal dual-sensor depth detection unit

Video and Graphics Processing
- Anti-flicker for output videos and graphics
- 1/15.5x to 16x video scaling
- 360° or 720° panoramic stitching of up to 6-channel videos
- 1/15.5x to 16x graphics scaling
- OSD overlaying of eight regions before encoding
- Video graphics overlaying of two layers (video layer and graphics layer)

ISP
- 2-channel independent ISP processing of video inputs from multiple sensors in TDM mode
- Adjustable 3A (AE, AWB, and AF) functions
- FPN removal
- Highlight suppression, backlight compensation, gamma correction, and color enhancement
- DPC, NR, and 6-DOF DIS
- 3DNR, image enhancement, and DCI
- Anti-fog
- LDC and fisheye correction
- Picture rotation by 90° or 270°
- Picture mirror and flip
- HDR10
- BT.2020 WCG
- Sensor built-in WDR, 4F/3F/2F frame-based/line-based WDR and local tone mapping
- ISP tuning tools for the PC

Audio Encoding and Decoding
- Voice encoding/decoding complying with multiple protocols by using software
- G.711, G.726, AAC, and other audio encoding formats
- Audio 3A (AEC, ANR, and ALC) functions

Security Engine
- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA1024/2048/3072/4096 signature verification algorithm implemented by using hardware
- HASH-SHA1/224/256/384/512 and HMAC_SHA1/224/256/384/512 tamper proofing algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and hardware random number generator

Video Interfaces
- VI interfaces
  - Eight sensor inputs
  - Maximum 32-megapixel (7680 x 4320) or 36-megapixel (6000 x 6000) resolution
  - 8-/12-/14-bit RGB Bayer DC timing VI, up to 150 MHz clock frequency
  - BT.601, BT.656, and BT.1120 VI interfaces
  - Maximum 16-lane MIPI/LVDS/sub-
LVDS/HiSPI/SLVS-EC interface for the serial sensor inputs
- Maximum 8-channel video inputs for the serial sensor inputs, supporting various working modes such as 1x16-lane/2x8-lane/4x4-lane/2x4-lane+4x2-lane/8x2Lane
- Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
- Programmable sensor clock output

Audio Interfaces
- Integrated audio codec, supporting 16-bit audio inputs and outputs
- I²S interface for connecting to the external audio codec
- Dual-channel differential MIC inputs for reducing background noises

Peripheral Interfaces
- POR
- External reset input
- Internal RTC
- Integrated 2-channel LSADC
- Five UART interfaces
- IR interface, I²C interface, SSP main interface, and GPIO interface
- Integrated two GMACs, supporting RGMII/RMII
- Two PWM interfaces
- Two SD 3.0/SDIO 3.0 interfaces and an SD 2.0 interface
- Two USB 3.0/USB 2.0 host/device ports
- 2-lane PCIe 2.0 RC/EP mode

External Memory Interfaces
- DDR4/LPDDR4 interface
  - 64-bit DDR4
  - 2x 32-bit LPDDR4 SDRAMs
  - Maximum capacity of 8 GB
- SPI NOR flash interface
  - 1-/2-/4-line mode
  - 3-byte or 4-byte address mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface
  - Maximum capacity of 512 MB
- NAND flash interface
  - 8-bit data width
  - SLC or MLC
  - 4-/8-/16-/24-/28-/40-/64-bit ECC
- eMMC 5.1 interface
  - Maximum capacity of 2 TB
- UFS 2.1 interface
  - Maximum capacity of 512 GB
- Booting from the SPI NOR flash, SPI NAND flash, or NAND flash
- Booting from an eMMC or UFS

SDK
- Linux SMP
- Linux+Huawei LiteOS dual-system AMP
- Client for the iOS and Android mobile phones, and high-performance H.265 decoding library

Physical Specifications
- Power Consumption
  - Typical power consumption of 3 W in 4K120 encoding mode
  - Multi-level power saving modes
- Operating voltages
  - 0.8 V core voltage
  - 1.8 V I/O voltage
  - 1.2 V DDR4 SDRAM interface voltage
  - 1.1 V LPDDR4 SDRAM interface voltage
- Package
  - RoHS, FC-CSP
  - Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.)
  - Lead pitch of 0.4 mm (0.02 in.)
Hi3559C V100

Hi3559C V100 Ultra-HD Mobile Camera SoC Brief Data Sheet

Functional Block Diagram

- 64bit DDR4/LPDD R4
- SDHC/XC
- SPI Nor/SPI Nand Flash
- Nand Flash
- UFS/eMMC
- USB2.0/3.0
- 2xLane PCIe2.0
- GE-PHY
- DDRC
- SDIO3.0 x2
- Flash I/F
- Nand I/F
- UFS/eMMC I/F
- USB 2.0/3.0 Host/Device
- PCIe2.0
- GMAC
- Audio CODEC
- I2S

ARM Subsystem
- Dual core Cortex A73 @1.8GHz
- Dual core Cortex A53 @1.2GHz
- Cortex A53 @1.2GHz

Image Subsystem
- GPU@MP2
- DSP/NNIE/IVE
- VPSS+VGS+GDC+AVSP
- IS (3A/WDR)
- MIPI/LVDS/HiSPI/SLVS-EC
- HDMI/LCD

Video Subsystem
- H.264 BP/MP/HP
- H.265 MP
- MJPEG/JPEG Encoder/Decoder

Sensor Hub
- Cortex M7 @192Mhz
- AES/DES/3DES
- RSA/HASH/TRNG OTP
- RSA/HASH
- TRNG

Audio Subsystem
- CODEC
- Audio

Hi3559CV100

RTC
- I2C
- SPI
- GPIOs
- IR
- UART
- PWM
- LSADC
Hi3559C V100 Mobile Camera and Professional Camera Solution

- Advanced 8K30 6-DOF video DIS
- 10-bit video, supporting HDR10
- Up to 10 Gbit/s rate of the 2-lane PCIe 2.0 interface, supporting 4K30 raw video output
- DDR4/LPDDR4 SDRAMs
- Two SDIO 3.0 interfaces, extended low-power Wi-Fi module, and the external SDXC card
- Dual MICs and advanced dual-MIC NR algorithm

Hi3559C V100 3D/VR Camera Solution

- Dual-channel 4K60fps input, 4-channel 3K x 3K input, or 8-channel 1080p input, supporting multi-channel hardware stitching
- 10-bit video, supporting HDR10
- DDR4/LPDDR4 SDRAMs
- Two SDIO 3.0 interfaces, extended low-power Wi-Fi module, and the external SDXC card
- Dual MICs and advanced dual-MIC NR algorithm
Hi3559C V100 Flying Camera Solution

- 6-DOF 4K60 video DIS in the gyro auxiliary information
- 10-bit video, supporting HDR10
- 4K30 raw video output
- DDR4/LPDDR4 SDRAMs
- Dual sensor inputs for bidirectional vision hovering and obstacle avoidance
- Various UART, I2C, and SPI interfaces for connecting the gyro, GPS, and barometer, implementing the flight control algorithm on Hi3559C V100
- 4-channel PWM signal outputs to the ESC
- Real-time HDMI video outputs for image transmission
### Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>3DES</td>
<td>triple data encryption standard</td>
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<tr>
<td>AAC</td>
<td>advanced audio coding</td>
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<tr>
<td>AE</td>
<td>automatic exposure</td>
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<tr>
<td>AEC</td>
<td>acoustic echo cancellation</td>
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<tr>
<td>AES</td>
<td>advanced encryption standard</td>
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<tr>
<td>AF</td>
<td>automatic focus</td>
</tr>
<tr>
<td>ALC</td>
<td>automatic level control</td>
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<tr>
<td>AMP</td>
<td>asymmetric multiprocessing</td>
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<tr>
<td>ANR</td>
<td>audio noise reduction</td>
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<tr>
<td>AVBR</td>
<td>adaptive variable bit rate</td>
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<tr>
<td>AWB</td>
<td>automatic white balance</td>
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<tr>
<td>CBR</td>
<td>constant bit rate</td>
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<tr>
<td>CMOS</td>
<td>complementary metal-oxide-semiconductor</td>
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<tr>
<td>codec</td>
<td>coder/decoder</td>
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<tr>
<td>DCI</td>
<td>dynamic contrast improvement</td>
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<tr>
<td>DDR</td>
<td>double data rate</td>
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<tr>
<td>DES</td>
<td>data encryption standard</td>
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<td>DIS</td>
<td>digital image stabilization</td>
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<td>DOF</td>
<td>degree of freedom</td>
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<td>DPC</td>
<td>defect pixel correction</td>
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<td>DRAM</td>
<td>dynamic random access memory</td>
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<td>DSI</td>
<td>display serial interface</td>
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<td>DSP</td>
<td>digital signal processor</td>
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<tr>
<td>eMMC</td>
<td>embedded multimedia card</td>
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<tr>
<td>EP</td>
<td>end point</td>
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<td>ESC</td>
<td>electronic speed control</td>
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<td>FPN</td>
<td>fixed pattern noise</td>
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<tr>
<td>FPU</td>
<td>floating-point unit</td>
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<td>RoHS</td>
<td>Restriction of Hazardous Substances</td>
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<tr>
<td>GMAC</td>
<td>Gigabit Ethernet Media Access Controller</td>
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<tr>
<td>GPIO</td>
<td>general-purpose input/output</td>
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<tr>
<td>GPS</td>
<td>Global Positioning System</td>
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<tr>
<td>GPU</td>
<td>graphics processing unit</td>
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<tr>
<td>HD</td>
<td>high definition</td>
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<tr>
<td>HMAC</td>
<td>hashed message authentication code</td>
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<tr>
<td>HDMI</td>
<td>high definition multimedia interface</td>
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<tr>
<td>HDR</td>
<td>high dynamic range</td>
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<tr>
<td>HiSPI</td>
<td>high-speed serial pixel interface</td>
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<tr>
<td>I2C</td>
<td>inter-integrated circuit</td>
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<tr>
<td>I2S</td>
<td>inter-IC sound</td>
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<tr>
<td>IR</td>
<td>infrared</td>
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<tr>
<td>ISP</td>
<td>image signal processor</td>
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<tr>
<td>LCD</td>
<td>liquid crystal display</td>
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<tr>
<td>LDC</td>
<td>lens distortion correction</td>
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<tr>
<td>LPDDR</td>
<td>low-power double data rate</td>
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<tr>
<td>LSADC</td>
<td>low-speed analog-to-digital converter</td>
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<tr>
<td>LVDS</td>
<td>low-voltage differential signaling</td>
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<tr>
<td>MIC</td>
<td>microphone</td>
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<tr>
<td>MIPI</td>
<td>mobile industry processor interface</td>
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<tr>
<td>MLC</td>
<td>multi-level cell</td>
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<tr>
<td>NNIE</td>
<td>Neural Network Inference Engine</td>
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<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>NR</td>
<td>noise reduction</td>
</tr>
<tr>
<td>OSD</td>
<td>on-screen display</td>
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<tr>
<td>OTP</td>
<td>one-time programming</td>
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<tr>
<td>PCIe</td>
<td>peripheral component interconnect express</td>
</tr>
<tr>
<td>PMC</td>
<td>power management controller</td>
</tr>
<tr>
<td>POR</td>
<td>power-on reset</td>
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<tr>
<td>PWM</td>
<td>pulse-width modulation</td>
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<tr>
<td>RC</td>
<td>root complex</td>
</tr>
<tr>
<td>RGB</td>
<td>red-green-blue</td>
</tr>
<tr>
<td>RGMII</td>
<td>reduced gigabit media independent interface</td>
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<tr>
<td>RoHS</td>
<td>Restriction of Hazardous Substances</td>
</tr>
<tr>
<td>ROI</td>
<td>region of interest</td>
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<tr>
<td>RSA</td>
<td>Rivest-Shamir-Adleman</td>
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<tr>
<td>RTC</td>
<td>real-time clock</td>
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<tr>
<td>SD</td>
<td>secure digital</td>
</tr>
<tr>
<td>SDIO</td>
<td>secure digital input/output</td>
</tr>
<tr>
<td>SDK</td>
<td>software development kit</td>
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<tr>
<td>SDRAM</td>
<td>synchronous dynamic random access memory</td>
</tr>
<tr>
<td>SDXC</td>
<td>secure digital extended capacity</td>
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<tr>
<td>SLC</td>
<td>single-level cell</td>
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<tr>
<td>SLVS-EC</td>
<td>Scalable Low Voltage Signaling interface with Embedded Clock</td>
</tr>
<tr>
<td>SoC</td>
<td>system-on-chip</td>
</tr>
<tr>
<td>SMP</td>
<td>symmetric multiprocessing</td>
</tr>
<tr>
<td>SPI</td>
<td>serial peripheral interface</td>
</tr>
<tr>
<td>SSP</td>
<td>synchronous serial port</td>
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<tr>
<td>SVP</td>
<td>Smart Vision Process</td>
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<tr>
<td>TDM</td>
<td>time division multiplexing</td>
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<tr>
<td>UART</td>
<td>universal asynchronous receiver transmitter</td>
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<tr>
<td>UFS</td>
<td>Universal Flash Storage</td>
</tr>
<tr>
<td>VBR</td>
<td>variable bit rate</td>
</tr>
<tr>
<td>VI</td>
<td>video input</td>
</tr>
<tr>
<td>VO</td>
<td>video output</td>
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<tr>
<td>VR</td>
<td>virtual reality</td>
</tr>
<tr>
<td>WCG</td>
<td>wide color gamut</td>
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<tr>
<td>WDR</td>
<td>wide dynamic range</td>
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